PATENT APPLICATION

In re application of:	Ji-Young Kim and Hyoung-Sub Kim		
Serial No.	Not yet assigned	Examiner:	Not yet assigned
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For:	INTEGRATION METHOD OF A SEMICONDUCTOR DEVICE HAVING A RECESSED GATE ELECTRODE		

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
_____	_____	6,063,669	5/16/2000	Takaishi		

FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name
_____	_____				

OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)

Examiner: _____

Date Considered: _____